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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,657	11/29/2001	Hiroshi Tamemoto	2936-0142P	2637

2292 7590 06/28/2004

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EXAMINER	
PERVEEN, REHANA	
ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,657	TAMEMOTO ET AL.	
	Examiner	Art Unit	
	Rehana Perveen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/01,7/02, 4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohara, Patent No. 6,600,575.

As to claim 1, Kohara teaches a clock supply circuit that supplies one or more clocks for driving one or more functional circuit blocks at a different frequency (col. 1 lines 22-33), a clock selector circuit that selects a clock being fed to each of the functional circuit blocks for each execution cycle (col. 2 lines 13-33), and the clock supply circuit and the clock selector circuit are configured so as to change an operating frequency or halt operation of the one or more functional circuit blocks for each execution cycle (col. 4 lines 37-65).

As to claim 2, Kohara teaches all of the limitations as stated above. In addition, Kohara also teaches an instruction decoder circuit that feeds a selection signal to the

clock selector circuit for selecting a most appropriate clock from one or more clocks by analyzing prescribed bits of an instruction code (decision circuit 11, col. 10 line 56 – col. 11 line 13).

As to claims 3 and 5, Kohara teaches all of the limitations as stated above. In addition, Kohara also teaches a memory select signal circuit that identifies a memory block to be accessed, and changing the operating frequency of one or more of the memory blocks in accordance with the performance of the memory block identified by the memory select signal circuit (reading function, figure 1).

As to claim 4, Kohara teaches all of the limitations as stated above. In addition, Kohara also teaches a I/O select signal circuit that identifies a peripheral circuit to be accessed, and changing the operating frequency of one or more of the peripheral circuits in accordance with the performance of the peripheral circuit identified by the I/O select signal circuit (printing function, figure 1).

Claims 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwazaki, Patent No. 6,073,244.

Iwazaki was cited as prior art in the Information Disclosure Statement filed on 7/18/2002.

As to claims 6 and 7, Iwazaki teaches a clock supply circuit that supplies one or more clocks for driving one or more functional circuit blocks at a different frequency, a clock selector circuit that selects a different clock being fed to each of the functional circuit blocks for each execution cycle, an analyzer circuit that analyzes instructions and feeds a selection signal to the clock selector circuit for selecting a most appropriate clock for each of the stages from one or more clocks, and the analyzer circuit analyzes and feeds the selection signal when the stages execute the instructions having a load different from each other, a stage executing an instruction having a lighter load is provided with a slower clock and the clock selection circuit selects a faster clock for heavier load (col. 3 line 48 – col. 4 line 61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwazaki, Patent No. 6,073,244, in view of Dowling, Patent No. 6,226,738.

As to claims 8 and 10, Iwazaki teaches all of the limitations as stated above in claims 6 and 7.

However, Iwazaki does not expressly teach a compiler that converts instructions into a VLIW format and assigns a most suitable clock to each of the instructions in accordance with content thereof to be processed, or a compiler that determines a most appropriate clock for each instruction according to content thereof and writes information thereof thus determined to prescribed bits of a compiled instruction code.

Dowling teaches a compiler that converts instructions into a VLIW format (col. 9 line 51 – col. 10 line 66) and assigns a most suitable clock to each of the instructions in accordance with content thereof to be processed, or a compiler that determines a most appropriate clock for each instruction according to content thereof and writes information thereof thus determined to prescribed bits of a compiled instruction code (col. 17 lines 30-49).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine teachings of Iwazaki and Dowling because Dowling's determination of most appropriate clock at compile time by the compiler, when incorporated into Iwazaki's system, would have enabled efficiency and throughput by issuing commands early to allow instruction preparation in advance.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwazaki, Patent No. 6,073,244, in view of Kapusta et al, Patent No. 5,799,176.

Iwazaki teaches all of the limitations as stated above in claim 6. However, Iwazaki does not expressly teach the clock selector circuit having a hierarchically arranged clock selector architecture in which clock branches are arranged hierarchically in accordance with frequency of use of the clocks.

Kapusta et al teach a clock selector circuit having a hierarchically arranged clock selector architecture in which clock branches are arranged hierarchically in accordance with frequency of use of the clocks (col. 5 lines 41-51 and col. 7 lines 5-18).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Iwazaki and Kapusta et al because Kapusta et al's clock selector arrangement, when incorporated into Iwazaki, would have enabled further efficiency and throughput by allowing reduced amount of time to select the appropriate clock.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rehana Perveen whose telephone number is 703-305-8476. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rehana Perveen
Primary Patent Examiner
Technology Center 2100